Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.016”**

**S/D**

**GATE**

**S/D**

**F26**

**GATE**

**.016”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GATE**

**Mask Ref: F26**

**APPROVED BY: DK DIE SIZE .016” X .016” DATE: 9/23/21**

**MFG: ZETEX THICKNESS .006” P/N: BF245C**

**DG 10.1.2**

#### Rev B, 7/19/02